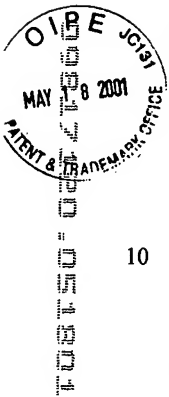


#4

**METHOD FOR MANUFACTURING DEVICE SUBSTRATE  
WITH METAL BACK-GATE AND STRUCTURE FORMED  
THEREBY**

**U.S. GOVERNMENT RIGHTS UNDER THE INVENTION**

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8908.



**CROSS-REFERENCE TO RELATED APPLICATION**

10 The present application is related to and claims priority from U.S. Provisional  
Patent Application No. 60/202,660, filed on May 8, 2000, to Chan et al., entitled  
“METHOD FOR MANUFACTURING DEVICE SUBSTRATE WITH METAL BACK-  
GATE AND STRUCTURE FORMED THEREBY”, assigned to the present assignee, and  
incorporated herein by reference.

## BACKGROUND OF THE INVENTION

### *Field of the Invention*

The present invention relates to a method for forming a device substrate and more particularly to a method for forming a device substrate with a metal back-gate and the structure formed thereby.

### *Description of the Related Art*

Laminating a thin metal layer (e.g., tungsten (W)) between silicon-based materials such as a gate oxide and a buried oxide is a key step to making substrates for double-gate devices with a metal back-gate. Because of its flexibility with all kinds of materials, even if the materials are polycrystalline, amorphous, or single crystalline but with very different lattice mismatch, wafer bonding is a promising approach to make this multilayer structure.

However, for the bonding process, after the room-temperature joining step, a thermal treatment at 1100°C is commonly used to enhance the bonding strength. Due to the weak adhesion at the interface between metals and silicon oxide as a result of their chemical and physical incompatibility such as thermal mismatch, the stacked layers are very likely to disintegrate during the high temperature bonding anneal in the form of delamination at weak interfaces. This problem has been observed experimentally and this conventional process is schematically shown in Figure 1. In the case of tungsten



improving the adhesion between these two incompatible materials with several innovative processes.

## **BRIEF DESCRIPTION OF THE DRAWINGS**

The foregoing and other purposes, aspects and advantages will be better understood from the following detailed description of a preferred embodiment of the invention with reference to the drawings, in which:

Figure 1 illustrates schematically a conventional processing;

Figure 2A illustrates schematically the process of the present invention;

Figure 2B illustrates a flow diagram of the inventive process;

10 Figures 3A-3C show the details of the process of Figure 2;

Figure 4 illustrates photographically a device silicon substrate with a tungsten backplane; and

Figure 5 illustrates analytical results of the process.

## **DETAILED DESCRIPTION OF PREFERRED EMBODIMENTS OF THE INVENTION**

Referring now to the drawings, and more particularly to Figures 2-5, there are shown preferred embodiments of the method and structures according to the present invention.

As mentioned above, the present invention resolves the above-mentioned and other problems of delamination between metals (e.g., W, TiN, etc.; W will be assumed in

the example described below) and low temperature oxide (LTO) during bonding anneal by improving the adhesion between these two incompatible materials with several innovative processes. As such, an 8" device substrate with W as the back-plane has been demonstrated for the first time, as shown in Figure 4 which is a photograph of the 8"

5 device substrate.

A key aspect of the method of the present invention is to use an intermediate "gluing" layer to enhance adhesion between multi-layers especially two layers with very different chemical and physical properties.

It is noted that this aspect can be well extended from a W back-gate to other  
10 metals or silicide (such as Ti-Nitride) back-gate substrates. Due to its readiness of forming silicide with metals and its compatibility with Si-based materials, a-Si is a desirable intermediate layer. Other intermediate layers may include silicon nitride, or poly-silicon. Further, it is noted that the intermediate layer could include the passivation layer as one of its layers, or the passivation layer could be used in addition to the  
15 intermediate layer(s).

The inventive process 200 is shown schematically in Figures 2A-2B and 3A-3C.

As described in further detail below, as shown in Figure 2B and Figure 3A, the method includes growing a thin gate oxide layer 302 on a SOI substrate 301 (e.g., having a thickness of about 500-750  $\mu\text{m}$  in a preferred application and including a silicon  
20 substrate 301a, an oxide 301b, and a SOI layer 301c) (step 210).

Then, in step 220, a physical vapor deposited (PVD) or chemical vapor deposited (CVD) metal 303 (e.g., tungsten, TiN, etc.; for ease of explanation below, the example of tungsten will be described) layer is deposited on the gate oxide. Preferably, the PVD/CVD metal 303 has a thickness sufficient to avoid leakage current and to

maintaining the integrity of the material. For example, the PVD/CVD metal 303 may have a thickness of about 20nm to about 500nm. Then, the PVD/CVD tungsten layer 303 is passivated. The passivation layer 305 preferably has a thickness of between about 0.2 to about 2 nm.

5 In step 225, intermediate gluing layer(s) 306 are formed on top of the passivated PVD/CVD W layer 303.

Thereafter, in step 230, an insulating material 304 such as a low temperature oxide (LTO) (AlOx, SiN, etc.; for ease of explanation, LTO will be assumed and described in the example below) is deposited on the W layer 303 and is smoothed with a  
10 chemical mechanical polishing (CMP).

As shown in Figure 3B, in step 240, the polished substrate with a multilayer stack is bonded to a monitor grade Si substrate 350 (e.g., approximately 750  $\mu\text{m}$  in thickness).

In step 250, the bonded structure is annealed at elevated temperatures to strengthen the bonding across the bonding interface.

15 The final 750  $\mu\text{m}$  SOI substrate with W ground plane is shown in Figure 3C and is achieved by polishing and wet etching processes. This composite substrate with buried tungsten ground plane can be utilized to fabricate nano-scale double gate SOI devices with metal gates.

It is noted that the PVD/CVD W layer 303 is passivated before the LTO  
20 deposition to prevent the reaction of W with oxygen and the subsequent delamination at the metal (W) 303 -LTO (which has a radical species such as OH or O, etc.) interface. The passivation of the PVD/CVD W layer 303 is preferably performed as described below.

In addition to the W passivation layer, several other intermediate layers have been tried to improve the compatibility of W and LTO. With the developed W passivation layer and intermediate layers, very good adhesion between W and SiO<sub>2</sub> layer is achieved and the multilayer structure remains intact during annealing at temperatures below 1100

5 C.

Thus, the inventive process contains three important aspects, as described in detail below, to achieve the above-mentioned and other advantages of the present invention.

As shown in Figures 2A-2B, a first important aspect is to form a thin W passivation layer after PVD/CVD W deposition (step 220).

10 The forming of the W passivation layer (e.g., cap) includes conducting an ultra high vacuum (UHV) desorption of native oxide on W under an atmosphere of approximately 10<sup>-9</sup> torr for 5 mm at approximately 750°C for about 5 min. Then, a monolayer of W-Si silicide is formed at approximately 625°C for approximately 1.5 min. reaction with SiH<sub>4</sub>. The bare W surface reacts with Si to form a monolayer of W-Si.

15 Thereafter, nitridation of W-Si occurs at about 750°C for about 30 min. with NH<sub>3</sub>. Active NH<sub>2</sub>, NH, species react with W-Si to form W-Si-N. This passivation layer has the structure of W-Si-N (e.g., see attached Auger Profile analysis results in Figure 5), and is effective in preventing W from being oxidized in the subsequent processing steps (e.g., see associated patent disclosure of "Method to Protect Refractory Metal Thin Films"

20 (U.S. Patent application No. \_\_/\_\_\_\_\_, having IBM Disclosure No. YOR8-1998-0774, incorporated herein by reference).

That is, Figure 5 shows a plot of the molar percent to the distance (sputter equivalent Å of SiO<sub>2</sub>). As shown in Figure 5, at the interface between the W and Co, on the surface of the passivated tungsten, there is a peak of silicon and nitrogen (Si, N, or Si-

N) which prevents the reaction of tungsten with oxygen. Thus, the benefit of using W as a passivation layer is evident. The monolayer of the intermediate layers serves to passivate the W to prevent any oxygen-containing species from reacting with the W.

Thus, adhesion must be improved and to do so, the invention employs a amorphous

- 5 silicon layer, a silicon nitride layer or a combination thereof, such that the temperature of the monolayer structure can withstand is significantly increased.

Thus, a second important aspect is to preferably insert intermediate layers such as a-Si,  $\text{Si}_3\text{N}_4$  or a combined layer of a-Si and  $\text{Si}_3\text{N}_4$  on top of an encapsulated W layer before the low temperature oxide (LTO) deposition (e.g., conducted at a temperature

- 10 between about 500 °C to about 750 °C). Preferably, to reduce thermal stress induced by the mismatch of thermal expansion coefficient between different materials, the fewer the number of intermediate layers, the better. Preferably, the intermediate layers have a thickness of about 3 nm to about 20 nm. These intermediate layers are more compatible with LTO layers due to their similar chemical composition than a metal material.

- 15 In addition, the thin a-Si or  $\text{Si}_3\text{N}_4$  intermediate layers will react with the PVD/CVD tungsten and form tungsten silicide during high temperature anneal (e.g., preferably conducted at a temperature within a range of about 300 °C to about 600 °C). Preferably the amorphous silicon layer has a thickness of at least 5 nm. The nitride layer would preferably have a thickness of at least 2 nm. Thin films are preferable.

- 20 Therefore, these intermediate layers serve as a "gluing" layer between a metal, such as W, and silicon oxide, in addition to the W-S-N passivation layer. As a result, the adhesion between W and the LTO is significantly enhanced. The improved adhesion is supported by the fact that 8" bonded wafers survived mechanical grinding process (e.g., approx. 320 grit on the first wheel and approx. 2000 grit on the second) and severe



chemical etching (e.g., 2 hours in 25% KOH solution at 80 °C). The W passivation layer preferably has a thickness of between about 0.2 nm to about 2 nm. It is noted that while the passivation layer is discussed above as containing nitrogen, a  $\text{SiC}_x$  layer or a  $\text{SiN}_x$  could be employed as the passivation layer.

- 5           The passivation layer can be provided separately from the intermediate glueing layer or can be a part thereof.

A third innovation of the present invention is to reduce the bonding anneal temperature from 1100°C to 650°C - 950°C (e.g., performed in step 250) . Low temperature bonding anneal has the combined benefits of keeping the W passivation layer

- 10 intact, maintaining the integrity of other materials especially the gate oxide, and minimizing the thermal stress in the multi-layer stack.

A thin layer of a-Si or BPSG (e.g., preferably having a thickness of about 3nm to about 10nm) with a lower flowing temperature can be used to enhance the bonding strength at bonding temperatures lower than 1100°C. Figures 2A and 3A-3C illustrate

- 15 the process of the invention schematically.

While the invention has been described in terms of a preferred embodiment, those skilled in the art will recognize that the invention can be practiced with modification within the spirit and scope of the appended claims.